I. REJECTIONS UNDER 35 U.S.C. § 102(e):

The Office Action has rejected claims 1 and 6 under 35 U.S.C. § 102(e) as being anticipated by *Feldner, et al.* (U.S. Patent No. 6,300,235) (hereinafter "*Feldner*"). Applicants respectfully traverse these rejections for at least the reasons provided below and respectfully request that the Examiner reconsider and withdraw these rejections.

Feldner does not disclose "*removing the ARC layer while reducing subsequent undesirable charge gain and subsequent undesirable charge loss over the use of a chemical mechanical polish in removing the ARC layer*" as recited in claim 1. The Examiner asserts that *Feldner* inherently discloses removing the ARC layer while reducing subsequent undesirable charge gain and subsequent undesirable charge loss over the use of a chemical mechanical polish in removing the ARC layer. Paper No. 7, page 3. Applicants respectfully contest the assertion that it is inherent that *Feldner* discloses *removing the ARC layer while reducing subsequent undesirable charge gain and subsequent undesirable charge loss over the use of a chemical mechanical polish in removing the ARC layer.* In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, in order for the Examiner to establish inherency, the Examiner must provide extrinsic evidence that must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999). Inherency, however, may not be established by probabilities or possibilities. *Id.* The mere fact that a certain thing may result from a given set of circumstances is not sufficient. *Id.* Thus, *Feldner* does not disclose all the limitations of claim 1, and thus *Feldner* does

anticipate claim 1. M.P.E.P. § 2131. Therefore, the Examiner must support the inherency argument with objective evidence meeting the above requirements.

For at least the above reasons, claim 1 is not anticipated by *Feldner*. Claim 6 recites combinations of features including the above combinations, and thus is not anticipated for at least the above reasons. Claims 6 recites additional features which, in combination with features of the claims upon which they depend, are not anticipated by *Feldner*.

For example, *Feldner* does not disclose "wherein the *lower layer includes a plurality of memory cells and is a first layer fabricated on the semiconductor device*" as recited in claim 6. The Examiner states that "*Feldner et al.* disclose the device represents a structure employed to fabricate a plurality of memory cells such as RAM, DRAM, and ROM (col. 4, 55-67)." Paper No. 7, page 3. Applicants traverse. Instead, *Feldner* discloses:

> FIG. 2A illustrates a cross sectional view of a structure 400 in accordance with one embodiment of the present invention. As shown, the structure comprises a substrate 412, such as silicon wafer. Other semiconductor substrates such as gallium arsenide, germanium, silicon on insulator (SOI), or other semiconductor materials are also useful. The substrate, for example, may be lightly or heavily doped with dopants of a pre-determined conductivity to achieve a desired electrical characteristics. The *structure, for example, represents a structure employed to fabricate devices such as transistors including nFETs or pFETs (field effect transistors) and other devices including capacitors and resistors*. Such devices, for example, are interconnected to form an integrated circuit (IC). Such IC includes a random access memory (RAM), a dynamic random access memory (DRAM), a synchronous DRAM (SDRAM), and a read only memory (ROM). Col. 4, lines 47-63 (emphasis added).

Thus, *Feldner* discloses a structure that may be employed to fabricate devices such as transistors and other devices including capacitors and resistors. Such devices, for example, are interconnected to form an integrated circuit where the integrated

circuit may include a RAM, a DRAM, an SDRAM or a ROM. This language does not disclose a *lower layer that includes a plurality of memory cells where the lower layer is fabricated on a semiconductor device and where an interlayer dielectric is provided on the lower layer.* Thus, *Feldner* does not disclose all the limitations of claim 6, and thus *Feldner* does not anticipate claim 6. M.P.E.P. § 2131.

As a result of the foregoing, Applicants respectfully assert that not each and every claim limitation was found within the cited prior art reference and thus claims 1 and 6 are not anticipated by *Feldner.*

It is noted that words are italicized only for emphasis. Words that are italicized are not meant to imply that only those words are not disclosed in the cited prior art.

II. REJECTIONS UNDER 35 U.S.C. § 103(a):

The Office Action has rejected claim 7 under 35 U.S.C. § 103(a) over *Feldner.* The Office Action has further rejected claims 2-3 under 35 U.S.C. § 103(a) as being unpatentable over *Feldner* in view of *Brooks et al.* (U.S. Patent No. 5,786,276) (hereinafter "*Brooks*"). The Office Action has further rejected claims 4-5 under 35 U.S.C. § 103(a) as being unpatentable over *Feldner* in view of *Wuu et al.* (U.S. Patent No. 6,222,214) (hereinafter "*Wuu*").

A. The Examiner Has Not Provided A *Prima Facie* Case Of Obviousness For Rejecting Claim 7.

Feldner does not teach or suggest "*providing a chemical mechanical polish of the conductive material*" as recited in claim 7. The Examiner states that "the chemical mechanical polish process is a well known process in the art." Paper No. 7, page 3. Assuming arguendo that a chemical mechanical process is well known in the

art, Applicants respectfully traverse the implied assertion that providing a chemical mechanical polish of the conductive material is well known in the art. Applicants respectfully request the Examiner to provide a reference that supports that Examiner's implied assertion pursuant to M.P.E.P. § 2144.03. Furthermore, the Examiner must submit **objective evidence** and not rely on his subjective opinion in support of modifying *Feldner* to provide a chemical mechanical polish of the conductive material. *In re Lee* 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Accordingly, one skilled in the art would not be able to recreate claim 7 in view of the cited prior art.

B. <u>The Examiner Has Not Provided A *Prima Facie* Case Of Obviousness For Rejecting Claims 2-3.</u>

A *prima facie* showing of obviousness requires the Examiner to establish, *inter alia*, that the prior art references teach or suggest, either alone or in combination, all of the limitations of the claimed invention, and the Examiner must provide a motivation or suggestion to combine or modify the prior art references to make the claimed inventions. M.P.E.P. §2142. The motivation or suggestion to combine references must come from one of three possible sources: the nature of the problem to be solved, the teaching of the prior art and the knowledge of persons of ordinary skill in the art. *In re Rouffet*, 47 U.S.P.Q.2d. 1453, 1458 (Fed. Cir. 1998). The showings must be clear and particular. *In re* Lee, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 50 U.S.P.Q.2d. 1614, 1617 (Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. *Id.*

In order to reject under 35 U.S.C. § 103, therefore, the Examiner must provide a proper motivation for combining or modifying the references. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1457-1458 (Fed. Cir. 1998). M.P.E.P. § 2142. The Examiner's motivation for modifying *Feldner* with *Brooks* to *remove the ARC layer using the*

plasma etch which utilizes a CH_3F/O_2 chemistry or a CHF_3/O_2 chemistry is "to use *CH_3F, CF_4 and O_2 mixture to dry plasma etch the ARC in order to yield faster rate.*" Paper No. 7, page 4.

There is no motivation to combine *Feldner* with *Brooks* as there is no suggestion or motivation in either *Feldner* or *Brooks* or in their combination or in the knowledge of those ordinarily skilled in the art to combine the teaching of *performing a dual damascene etch through a layer stack disposed above a substrate* as taught in *Feldner* with the teaching of a *chemical downstream etching (CDE) that is selective to silicon nitrides (SiN) over silicon oxides (SiO)* as taught in *Brooks*. *Feldner* teaches:

> The organic ARC layer 513 may be etched by placing the wafer in an oxide etch chamber where a first etch process known in the art as RIE utilizing N_2 etchant source gas breaks through the organic ARC layer 513 in the areas exposed by the developed photoresist. Col. 6, lines 54-57.

Thus, *Feldner* teaches etching an ARC layer using a process known in the art as RIE. *Brooks* teaches that:

> As a result of such drawbacks, a number of workers in the field have begun to use dry plasma etching of silicon nitride instead of wet etching. Dry plasma etching often uses disassociated radicals of fluorine or of other halogens for etching quickly through the otherwise difficult-to-cut silicone nitride material. Col. 2, lines 31-36.

Brooks further teaches that:

> In accordance with a first aspect of the invention, one or both of the gaseous compounds, CH_3F (methyl fluoride) and CH_2F_2 (ethyl difluoride) are used in combination with CF_4 (carbon tetrafluoride) and O_2 (oxygen) to create a remote plasma. A downstream output (afterglow) of the plasma is applied to a wafer or other like workpiece that has exposed silicon nitride adjacent to exposed silicon oxide and/or exposed silicon. Col. 2, lines 57-64.

Brooks further teaches that:

> Wafer backside Helium cooling pressure: 8 Torr. The central recipe point of Table 1A has been found to exhibit SIN etch rates of about 2400 A/min or higher and selectively for nitride over nitride of about 60 to 1 or greater. Col. 3, lines 20-23.

Thus, *Brooks* teaches dry plasma etching through the otherwise difficult to cut ***silicon nitride material*** using a mixture of CH_3F (methyl fluoride) in combination with CF_4 (carbon tetrafluoride) and O_2 (oxygen). The Examiner does not show why the teaching of *performing a dual damascene etch through a layer stack disposed above a substrate* as taught in *Feldner* is combined with the teaching of a *chemical downstream etching (CDE) that is selective to silicon nitrides (SiN) over silicon oxides (SiO)* as taught in *Brooks* from either *the nature of the problem to be solved, the teaching in the prior are or the knowledge of persons of ordinary skill in the art. In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998). The Examiner must provide **objective** evidence for combining *Feldner* which teaches *performing a dual damascene etch through a layer stack disposed above a substrate* with *Brooks* which teaches *chemical downstream etching (CDE) that is selective to silicon nitrides (SiN) over silicon oxides (SiO).*

As stated above, the Examiner's motivation for modifying *Feldner* with *Brooks* to *remove the ARC layer using the plasma etch which utilizes a CH_3F/O_2 chemistry or a CHF_3/O_2 chemistry* is so that *Feldner* can *use CH_3F, CF_4 and O_2 mixture to dry plasma etch the ARC in order to yield faster rate.* However, ***Feldner does not teach etching silicon nitride**, but instead teaches etching ARC layer 513.* The Examiner has not shown why *Feldner* should be modified to ***etch silicon nitride*** from either *the nature of the problem to be solved, the teachings of the prior art or in the knowledge of persons of ordinary skill in the art. In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998). Further, the Examiner has not shown why *Feldner* should be modified with *Brooks* to use a CH_3F, CF_4 and O_2 mixture to dry plasma

etch the ARC in order to yield faster rate from either the *nature of the problem to be solved, the teachings of the prior art or in the knowledge of persons of ordinary skill in the art. Id.* Furthermore, the Examiner has not shown why *Feldner* should be modified with *Brooks* to *remove the ARC layer using the plasma etch which utilizes a CH_3F/O_2 chemistry or a CHF_3/O_2 chemistry* from either *the nature of the problem to be solved, the teaching of the prior art, or the knowledge of persons of ordinary skill in the art. Id.* The Examiner must submit **objective evidence** and not rely on his subjective opinion in support of modifying *Feldner* with *Brooks* to etch silicon nitride as taught in *Brooks. In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Further, the Examiner must submit **objective evidence** and not rely on his subjective opinion in support of modifying *Feldner* to use CH_3F, CF_4 and O_2 mixture to dry plasma etch the ARC in order to yield faster rate. *Id.* Further, the Examiner must submit **objective evidence** and not rely on his subjective opinion in support of modifying *Feldner* with *Brooks* to *remove the ARC layer using a plasma etch where a plasma etch utilizes a CH_3F/O_2 chemistry or a CHF_3/O_2 chemistry. Id.* Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 2-3.

C. *Feldner* and *Brooks*, Taken Singly or in Combination, Do Not Teach or Suggest the Limitations of Claims 2-3.

Feldner and *Brooks,* taken singly or in combination, do not teach or suggest "*removing the ARC layer using the plasma etch*" as recited in claim 2. Furthermore, *Feldner* and *Brooks*, taken singly or in combination, do not teach or suggest "wherein the plasma etch further *utilizes a CH_3F/O_2 chemistry or a CHF_3/O_2 chemistry*" as recited in claim 3. The Examiner states that *Brooks* "disclose a plasma etching processing (*Brooks* col. 2, lines 50-54) using a mixture of methyl fluoride (CH_3F), carbon tetrafluoride (CF_4) and oxygen (O_2) to remove the ARC." Paper No. 7, page 4. Instead, *Brooks* teaches:

> As a result of such drawbacks, a number of workers in the field have begun to use dry plasma etching of silicon nitride instead of wet etching. Dry plasma etching often uses disassociated radicals of fluorine or of other halogens for etching quickly through the otherwise difficult-to-cut silicone nitride material. Col. 2, lines 31-36.

Brooks further teaches that:

> In accordance with a first aspect of the invention, one or both of the gaseous compounds, CH_3F (methyl fluoride) and CH_2F_2 (ethyl difluoride) are used in combination with CF_4 (carbon tetrafluoride) and O_2 (oxygen) to create a remote plasma. A downstream output (afterglow) of the plasma is applied to a wafer or other like workpiece that has exposed silicon nitride adjacent to exposed silicon oxide and/or exposed silicon. Col. 2, lines 57-64.

Brooks further teaches that:

> Wafer backside Helium cooling pressure: 8 Torr. The central recipe point of Table 1A has been found to exhibit SIN etch rates of about 2400 A/min or higher and selectively for nitride over nitride of about 60 to 1 or greater. Col. 3, lines 20-23.

Thus, *Brooks* teaches dry plasma etching *silicon nitride material* using one or both of the gaseous compounds CH_3F and CH_2F_2 in combination with CF_4 and O_2. Hence, *Brooks* does not teach or suggest *removing an ARC layer using a plasma etch* but instead *teaches etching difficult-to-cut silicon nitride material.* Furthermore, *Brooks* does not teach or suggest plasma etch *using a CH_3F/O_2 chemistry or a CHF_3/O_2 chemistry.* Instead, *Brooks* teaches *using one or both of the gaseous compounds CH_3F and CH_2F_2 in combination with CF_4 and O_2.* Accordingly, one skilled in the art would not be able to recreate claims 2 and 3 in view of the cited prior art.

D. **The Examiner Has Not Established A *Prima Facie* Case of Obviousness For Rejecting Claims 4-5.**

As stated above, a *prima facie* showing of obviousness requires the Examiner to establish, *inter alia*, that the prior art references teach or suggest, either alone or in combination, all of the limitations of the claimed invention, and the Examiner must provide a motivation or suggestion to combine or modify the prior art reference to make the claimed inventions. M.P.E.P. §2142. The motivation or suggestion to combine references must come from one of three possible sources: the nature of the problem to be solved, the teaching of the prior art and the knowledge of persons of ordinary skill in the art. *In re Rouffet*, 47 U.S.P.Q.2d. 1453,1458 (Fed. Cir. 1998). The showings must be clear and particular. *In re* Lee, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 50 U.S.P.Q.2d. 1614, 1617 (Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. *Id.*

In order to reject under 35 U.S.C. § 103, therefore, the Examiner must provide a proper motivation for combining or modifying the references. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1457-1458 (Fed. Cir. 1998); M.P.E.P. § 2141. The Examiner does not provide any objective motivation for modifying *Feldner* with *Wuu* to fill the plurality of via holes with tungsten. Paper No. 7, page 4. All the Examiner provides is his own subjective opinion which does not amount to the required objective evidence. Further, the Examiner's motivation for modifying *Feldner* with *Wuu* to provide an interlayer dielectric that is BPTEOS is "in order to apply it easily and it is good barrier layer." Paper No. 7, page 5. Again, this is a subjective opinion and not objective evidence.

There is no motivation to combine *Feldner* with *Wuu* as there is no suggestion or motivation in either *Feldner* or *Wuu* or in their combination or in the knowledge of those ordinarily skilled in the art to combine the teaching of *performing a dual*

damascene etch through a layer stack disposed above a substrate as taught in *Feldner* with the teaching of *fabricating a novel plug structure for low resistance ohmic stacked contacts and at the same time forming metal contacts to devices on a SRAM cell* as taught in *Wuu*. As stated above, *Feldner* teaches performing a dual damascene etch through a layer stack disposed above a substrate. *Wuu* teaches that:

> [a] method for fabricating a novel plug structure for low resistance ohmic stacked contacts and at the same time forming metal contacts to devices on a SRAM cell. Abstract.

Thus, *Wuu* teaches *fabricating a novel plug structure for low resistance ohmic stacked contacts and at the same time forming metal contacts to devices on a SRAM cell*. The Examiner has not objectively show why the teaching of *performing a dual damascene etch through a layer stack disposed above a substrate* as taught in *Feldner* is combined with the teaching of *fabricating a novel plug structure for low resistance ohmic stacked contacts and at the same time forming metal contacts to devices on a SRAM cell* as taught in *Wuu* from either *the nature of the problem to be solved, the teaching in the prior are or the knowledge of persons of ordinary skill in the art. In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998). The Examiner must provide **objective** evidence for combining *Feldner* which teaches *performing a dual damascene etch through a layer stack disposed above a substrate* with *Wuu* which teaches *fabricating a novel plug structure for low resistance ohmic stacked contacts and at the same time forming metal contacts to devices on a SRAM cell.*

As stated above, the Examiner does not provide any objective motivation for modifying *Feldner* with *Wuu* to fill the plurality of via holes with tungsten. Paper No. 7, page 4. The Examiner has not objectively shown why *Feldner* should be modified to fill the via holes with tungsten from either *the nature of the problem to be solved, the teaching of the prior art, or the knowledge of persons of ordinary skill in the art. In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998). Instead, the Examiner states that "tungsten is a common material used to create a contact plug,

such as disclosed in *Wuu et al.* (*Wuu*, Col. 7, lines 12-13). Therefore, it would have been obvious to use tungsten to fill the plurality of via holes." Paper No. 7, page 4. The Examiner must submit **objective evidence** and not rely on his subjective opinion in support of modifying *Feldner* to fill via holes with tungsten. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002).

Furthermore, as stated above, the Examiner's motivation for modifying *Feldner* with *Wuu* to provide an interlayer dielectric that is BPTEOS is "in order to apply it easily and it is good barrier layer." Paper No. 7, page 5. *Wuu* teaches that:

> [a] third insulating layer 22 is deposited over the patterned layer 18, as also shown in FIG. 7. Preferably the insulating layer is composed of a low flow glass to provide a leveling effect for planarizing the surface. For example, layer 22 can be deposited by low pressure chemical vapor deposition (LPCVD) reactor by decomposing a tetraethosiloxane (TEOS) while introducing dopants such as phosphine (PH_3) and diborane(6) (B_2H_6) to form the BPTEOS glass. The glass is then annealed for about between 15 to 60 minutes at a temperature of between about 800 to 900° C to level the glass layer 22. The *layer also serves as a barrier layer to sodium (Na) contamination.* Col. 6, lines 32-44.

Hence, ***Wuu* teaches depositing layer 22 to serve as a barrier layer to sodium (Na) contamination**. The Examiner has not objectively shown why Feldner should be modified with *Wuu to deposit a layer that serves as a barrier layer to sodium contamination* from either *the nature of the problem to be solved, the teaching of the prior art, or the knowledge of persons of ordinary skill in the art. In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998). Further, the Examiner has not objectively shown why *Feldner* should be modified with *Wuu* to *provide an interlayer dielectric on the lower level that is BPTEOS* from either *the nature of the problem to be solved, the teaching of the prior art, or the knowledge of persons of ordinary skill in the art. Id.* The Examiner must submit **objective evidence** and not rely on his subjective opinion in support of modifying *Feldner to deposit a layer that serves as a barrier layer to sodium contamination. In re Lee*, 61 U.S.P.Q.2d 1430,

1434 (Fed. Cir. 2002). Further, the Examiner must submit **objective evidence** and not rely on his subjective opinion in support of modifying *Feldner* to *provide an interlayer dielectric on the lower level that is BPTEOS. Id.* Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 4-5.

E. *Feldner* and *Wuu*, Taken Singly or in Combination, do not Teach or Suggest the Limitations of Claim 5.

Feldner and *Wuu*, taken singly or in combination, do not teach or suggest "*wherein the interlayer dielectric is BPTEOS*" as recited in claim 5. The Examiner states that "*Feldner* et al. do not disclose the interlayer dielectric is BPTEOS. However, *Wuu* et al. disclose a method of forming metal contacts in a semiconductor device utilizing BPTEOS as interlayer dielectric layer (*Wuu* col. 6, lines 32-44). *Wuu* et al. teach that BPTEOS is a low flow glass and a good barrier layer (*Wuu* col. 6, lines 32-44)." Paper No. 7, page 5. Instead, *Wuu* teaches:

> [a] third insulating layer 22 is deposited over the patterned layer 18, as also shown in FIG. 7. Preferably the insulating layer is composed of a low flow glass to provide a leveling effect for planarizing the surface. For example, layer 22 can be deposited by low pressure chemical vapor deposition (LPCVD) reactor by decomposing a tetraethosiloxane (TEOS) while introducing dopants such as phosphine (PH_3) and diborane(6) (B_2H_6) to form the BPTEOS glass. The glass is then annealed for about between 15 to 60 minutes at a temperature of between about 800 to 900° C to level the glass layer 22. The *layer also serves as a barrier layer to sodium (Na) contamination.* Col. 6, lines 32-44.

Thus, *Wuu* teaches a third insulating layer 22 (Figure 7 of *Wuu*) on top of patterned layer 18 (Figure 7 of *Wuu*) and second insulating layer 16 (Figure 7 of *Wuu*) where the third insulating layer 22 (BPTEOS glass) may be used to *serve as a barrier layer to sodium contamination.* This language does not teach or suggest that *layer 22 is an interlayer* dielectric. Accordingly, one skilled in the art would not be able to recreate claim 5 in view of the cited prior art.

F. **Conclusion.**

As a result of the foregoing, Applicants respectfully assert that the Examiner's *prima facie* case of obviousness is not taught or suggested by the cited prior art since there are numerous claim limitations not taught or suggested in the cited prior art, and thus one skilled in the art would not have been able to recreate claims 2-5 and 7 in view of the cited prior art.

It is noted that words are italicized only for emphasis. Italicizing is not meant to imply that only those words that are italicized are not taught or suggested in the cited prior art.

III. CONCLUSION:

As a result of the foregoing, it is asserted by Applicants that claims 1-7 in the Application are in condition for allowance, and respectfully request an early allowance of such claims.

Applicants respectfully request that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining problems.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

The paragraph beginning at line 2 of page 11 has been amended as follows:

Figure 5B depicts the semiconductor device 200 after step 110 or 122, removal of the ARC layer 232. A second layer of components can be fabricated on the ILD 230 [232]. Because the ARC layer 232 has been removed, the memory cells 210 and 220 can be erased using UV light. Moreover, the CMP step was omitted in lieu of, for example, a plasma etch. Thus, the unanticipated charge gain or unanticipated charge loss are reduced beyond that achieved using conventional CMP for removing the ARC layer 232.

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